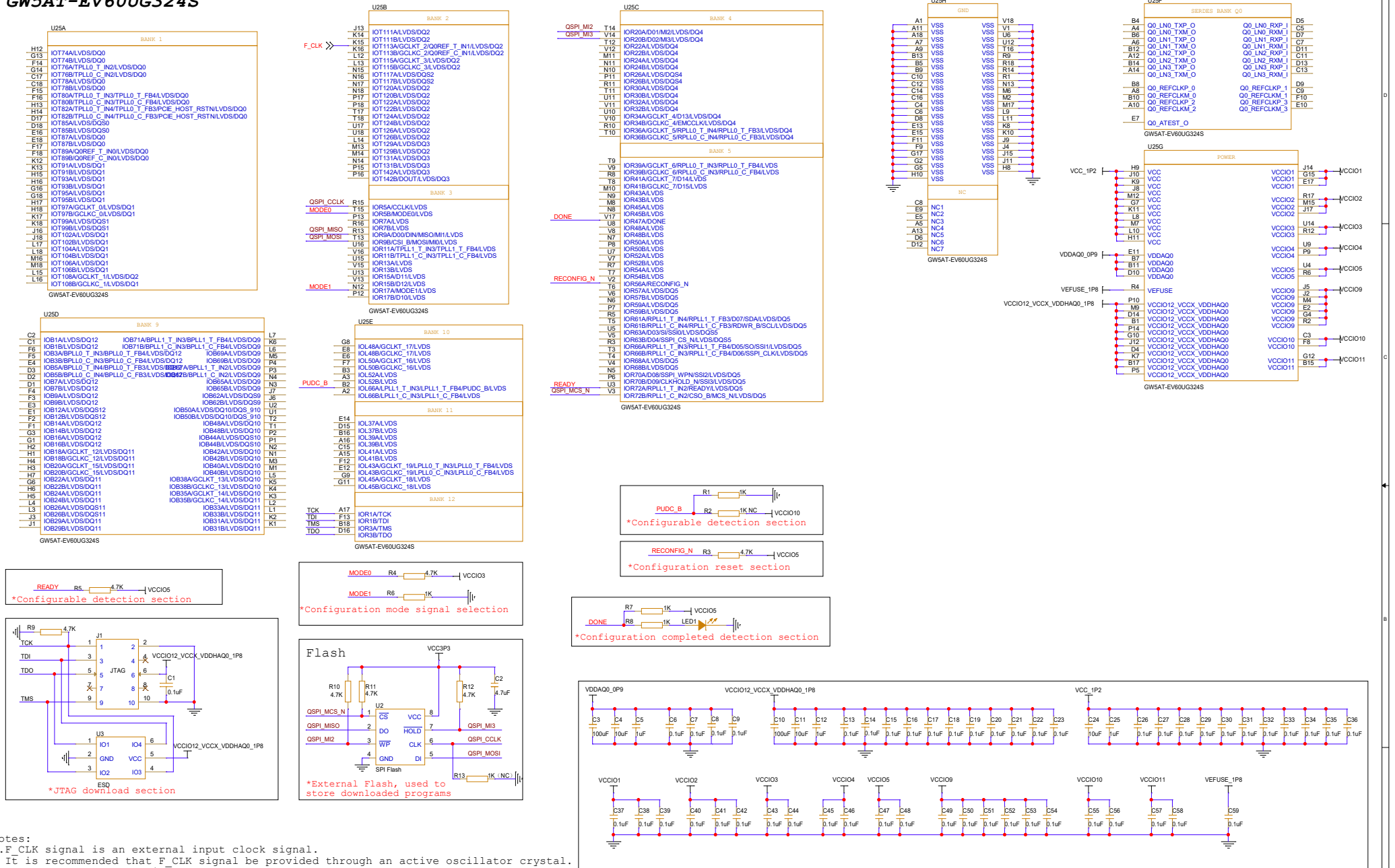


GW5AT-60K POWER SPEC

名称	描述	最小值	最大值
FPGA Logic			
V _{CC}	核电压, LV	0.93V	1.03V
	核电压, EV	1.14V	1.89V
V _{CCIO}	I/O Bank电压	1V	3.465V
V _{CCX} ^[1]	辅助电压	1.71V	3.465V
V _{EFUSE} ^{[2][3]}	eFuse写入所需电压	1.62V	1.98V
Gigabit Transceiver			
V _{DDHAQ*}	QUAD*内部高压供电电压	1.71V	1.89V
V _{DDAQ*}	QUAD*内部模拟电路供电电压	0.87V	1.03V
V _{DDTQ*}	QUAD* TX发送端供电电压	0.87V	1.03V
V _{DDDQ*}	QUAD*内部数字电路供电电压	0.87V	1.03V
MIPI			
V _{DDAM}	MIPI模块模拟电路供电电压	0.87V	1.08V
V _{DDXM}	MIPI模块模拟辅助供电电压	1.71V	3.465V
V _{DDDM}	MIPI模块数字电路供电电压	0.87V	1.08V
V _{DD12M}	MIPI模块LP模式供电电压	1.14V	1.32V
ADC			
V _{CCADC}	ADC模块供电电压	1.62V	1.98V
V _{REFN}	ADC模块参考电压	0V	0V
V _{REFP}	ADC模块参考电压	0V	1.25V
注！			
^[1] 当需要使用内部差分端接电阻时，V _{CCX} 必须大于等于3V；V _{CCX} =1.8V时，IO输入输出的F _{max} 会受到限制，对于F _{max} >600Mbps的输入输出应用，V _{CCX} 需要大于等于2.5V。			
^[2] 当不需要写eFuse的时候，这个电源可以接GND或floating。			
^[3] 当需要写eFuse的时候（如AES key写入，Multiboot相关的golden image的启动地址变更等），请检查并确认V _{EFUSE} 管脚的电压已正确设置为1.8V。			
若某些封装或者PCB上多个电源短接，需要取所有短接电源范围的交集，同时满足多个电源的需求。			

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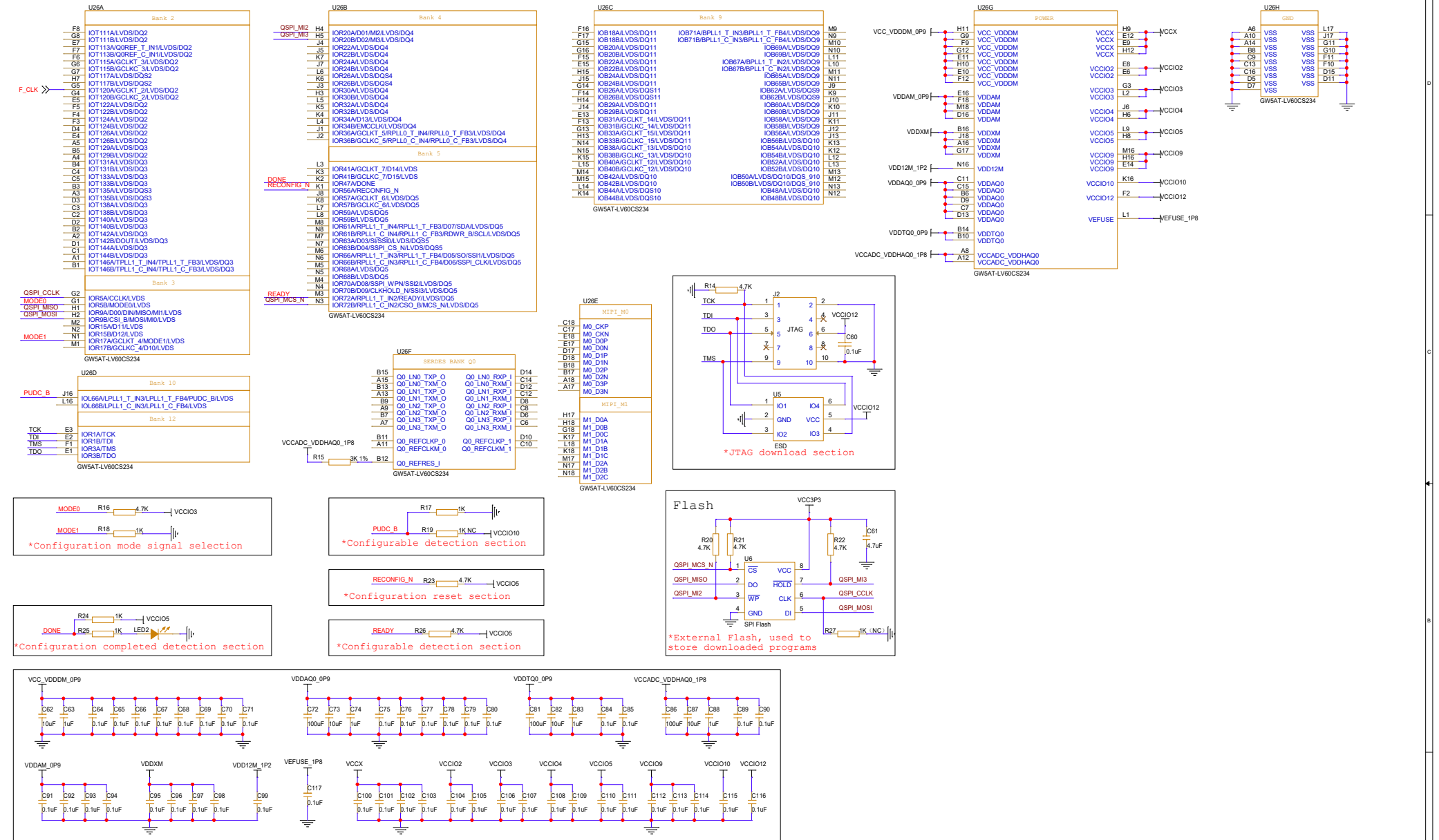


Notes:

- 1.F CLK signal is an external input clock signal.
- 2.External Flash memory is used to store downloaded programs.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- 6.This package does not support the use of internal differential termination resistors.
- 7.The MSPI signal levels must match the Flash power supply voltage.
- 8.If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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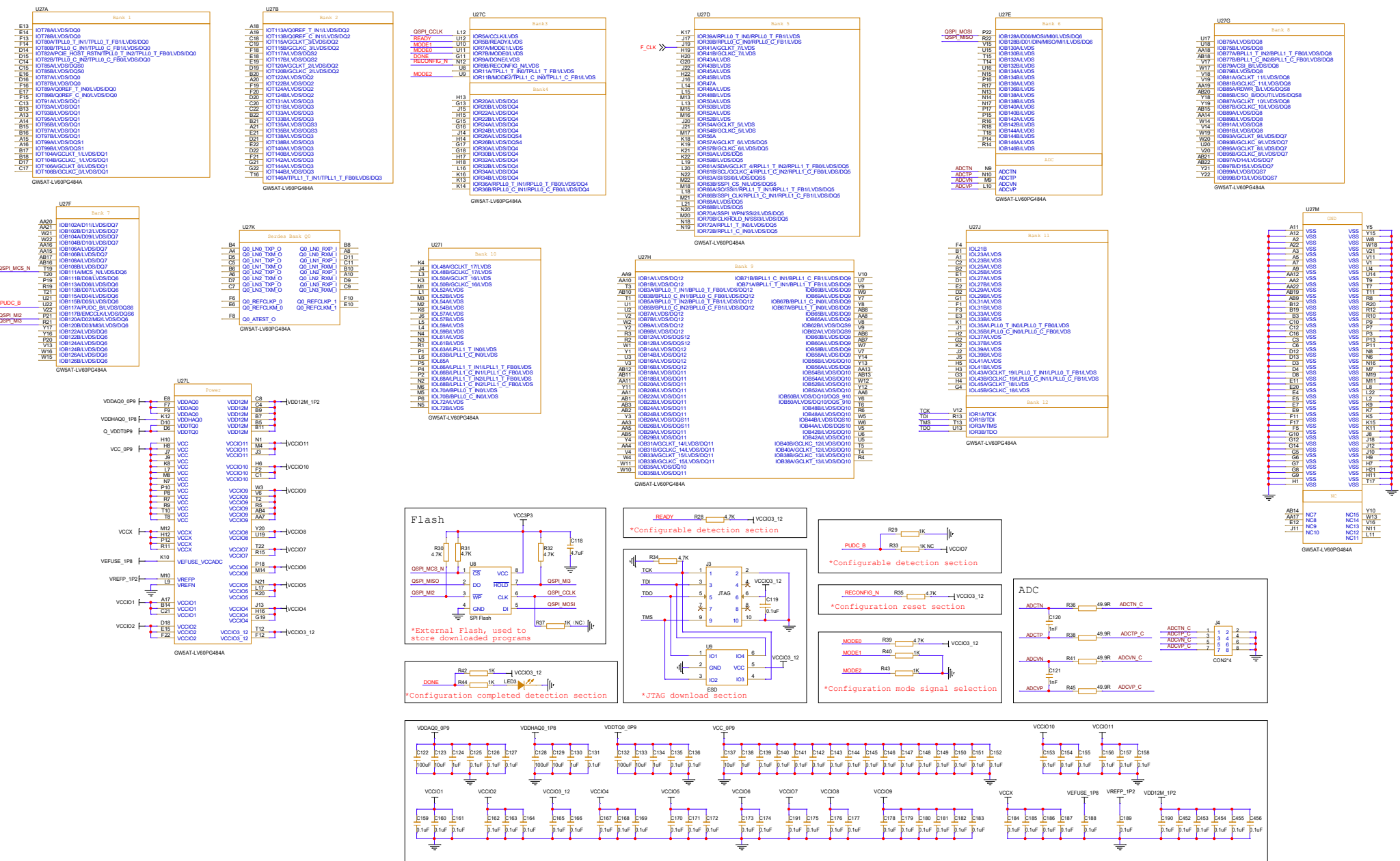


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title		
GOWIN Minimum System Diagram		
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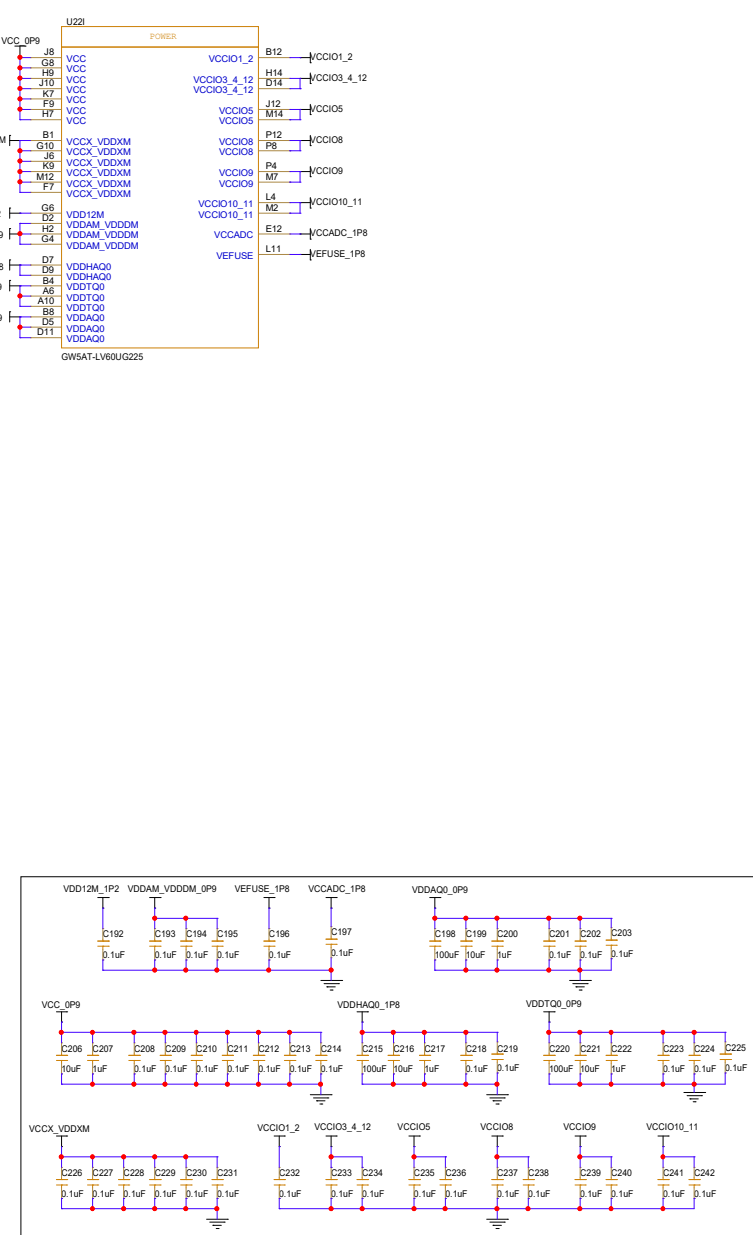
GW5AT-LV60PG484A



Notes:

- 1.F CLK signal is an external input clock signal.
 - It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
 - For details about SPI Flash mode selection, see "Chapter 4: SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
 - For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.
 - If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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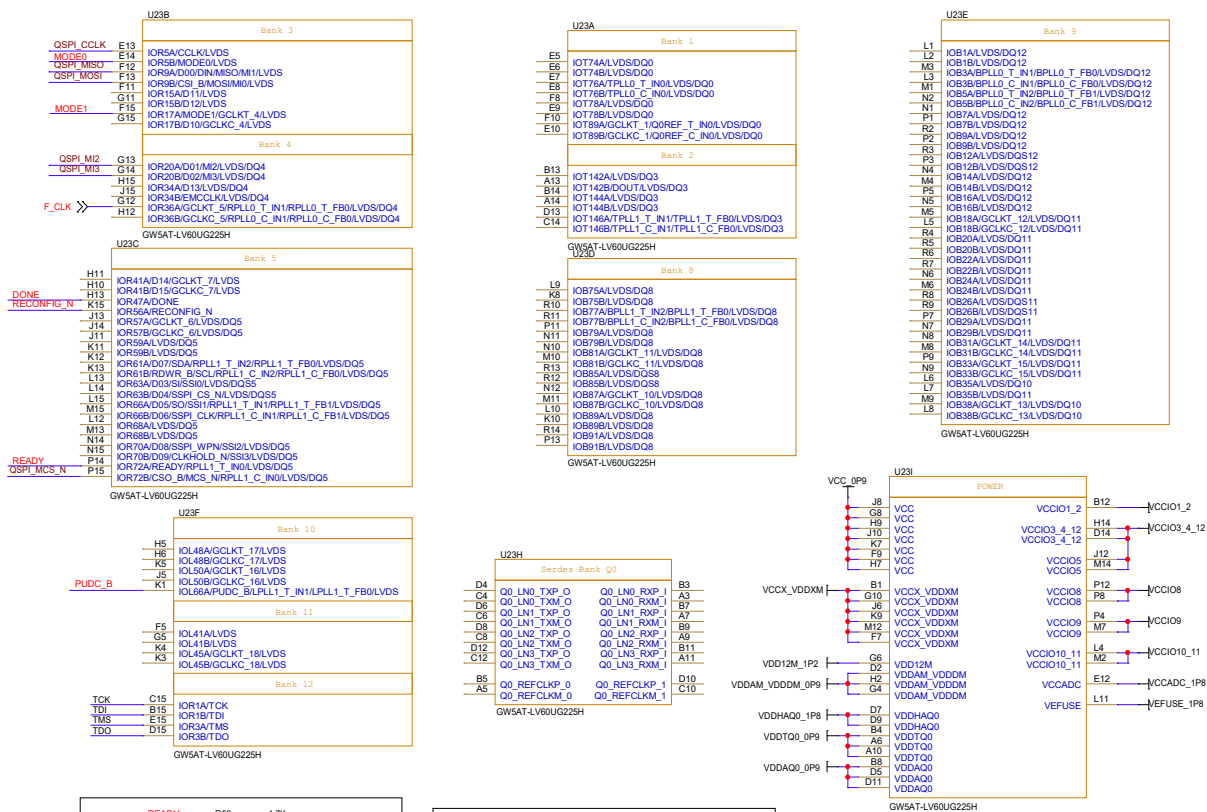


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

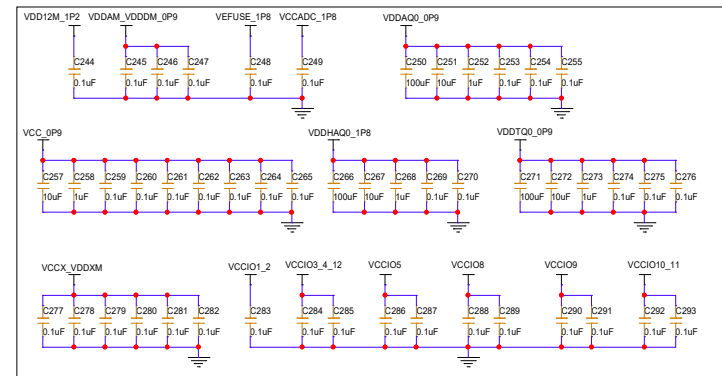
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GOWIN Minimum System Diagram				
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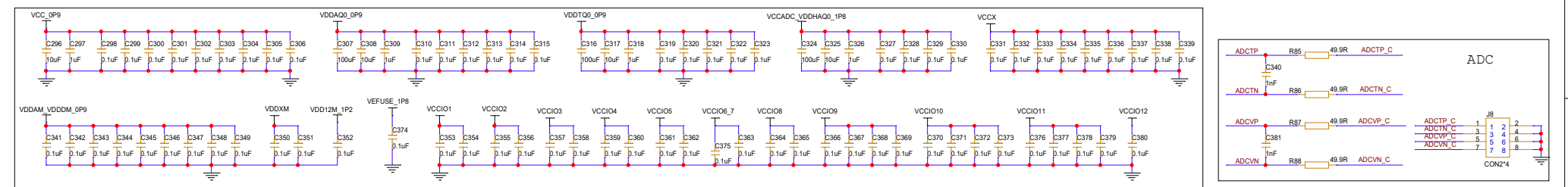
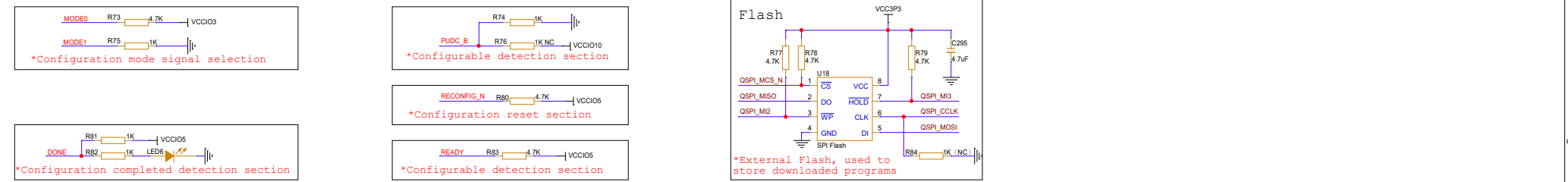
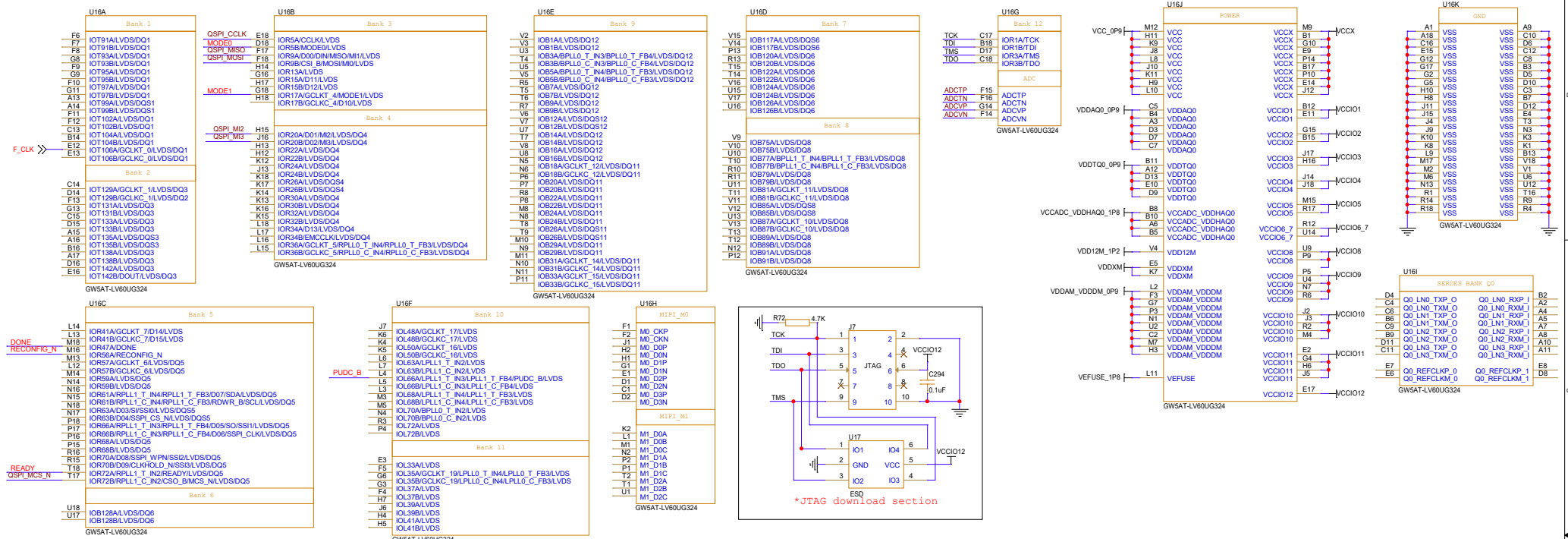
Notes:

- 1.F CLK signal is an external input clock signal.
 - 2.External Flash memory is used to store downloaded programs.
 - 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
 - 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
 - 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



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GOWIN Minimum System Diagram		
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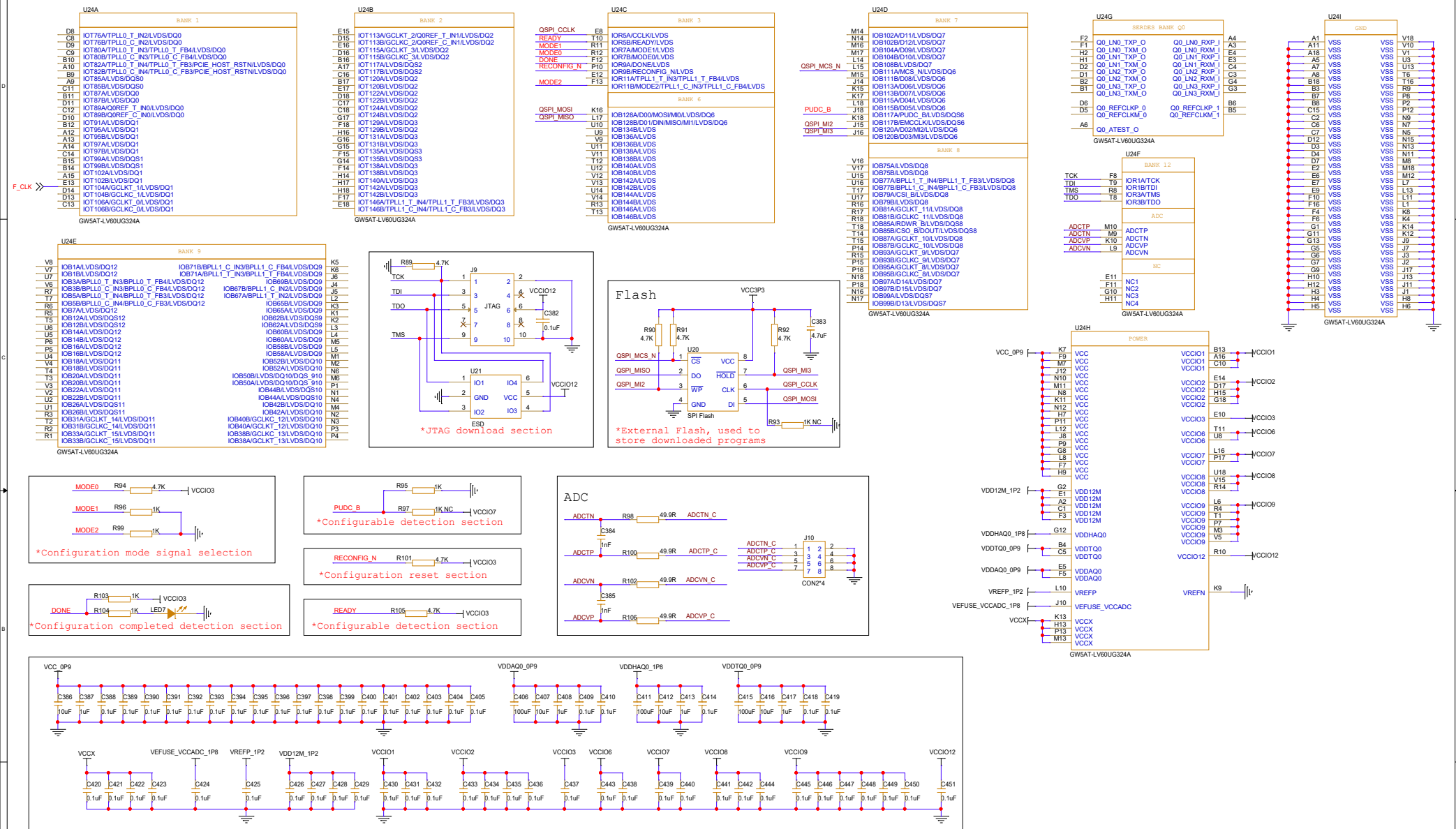
Notes:

- 1.F CLK signal is an external input clock signal.
- 2.External Flash memory is used to store downloaded programs.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- 6.The MSPI signal levels must match the Flash power supply voltage.

If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718, Arora V 60K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.